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Cascaded H-Bridge Multilevel Inverter Using Micro-Controller for Single Phase Induction Motor

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ABSTRACT: This paper presents a micro controller based control of multilevel inverter for single phase Induction motor. IGBT is used as power element. Pulse width modulation techniques (PWM), introduced three decades ago, are the most used methods to control the voltage and frequency supplied to electrical AC machines. This work proposes a new switching scheme for the cascaded H-Bridge multilevel inverter. Unlike other schemes, the proposed method is based on the symmetric regular sampling PWM with a single carrier and multiple modulating signals. On-transcendental trigonometric equations that define the switching instants of the multilevel inverter are derived [19]. This algorithm is implemented by a low-cost fixed-point microcontroller on an experimental five level cascaded inverter test-rig. Multilevel inverter has gained attention in recent years due to its high power capability associated with lower output harmonics. Several multilevel topologies have been reported in the literature and this paper focuses on asymmetric cascaded PWM technique. This technique provides reduced harmonics in the output voltage and significantly improves the RMS value of the output voltage compared to the conventional Sinusoidal Pulse Width Modulation (SPWM). A detailed study of the proposed modulation technique is carried out five-level PWM inverter test rig has been built to implement the proposed algorithm. Gating signals are generated using PIC microcontroller. The performance of the inverter has been analyzed and compared with the result obtained from theory. A scheme based on 5-level PWM inverter, which control a high performance 8-bit standard microcontroller with gate driver circuit and additional hardware is used, which allows a flexible and economical solution. The output voltage can be varied in a large range and with a good resolution. Experimental data obtained from an induction motor drive will be presented.

Keywords: PWM, PIC micro-controller, multilevel inverter, induction motor.

I. INTRODUCTION

Multilevel inverters have very important development for high power medium voltage AC drives. Quite a lot of topologies have found industrial approval [49];
a. Neutral Point Clamped Multilevel Inverter.
b. Flying capacitor Multilevel Inverter.
c. Cascaded Multilevel Inverter.
Maynard and Foch introduced a flying-capacitor-based inverter in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The cascaded multilevel inverters offer more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, at low switching frequency, higher efficiency, and lower voltage rating devices. An important question in designing an effective multilevel inverter is to ensure that, the total harmonic distortion (THD) in the output voltage waveform is small. A complete solution is obtainable for computing all possible switching angles that achieve the required fundamental voltages and eliminate the lower order harmonics [1]. On the other hand, it was assumed that the dc sources were all equal, which will probably not be the case in applications even if the sources are nominally unequal. Here, it is shown how the method in [2] can be extended to two unequal dc source inverter. Particularly, eliminating harmonics in a multilevel converter in which the separate dc sources do not have equal voltage levels is measured. Normally each phase of a cascaded multilevel converter requires n DC sources for 2n+1 levels. For many applications, to get several separate DC sources is difficult, and too many DC sources will be necessary many long cables and might lead to voltage unbalance among the DC sources. To reduce the number of DC sources necessary while the cascaded H-bridge multilevel converter is applied to a motor drive, a scheme is proposed in [3] that allow the use of two unequal DC sources to generate five level equal step multilevel inverter output. In this paper, the lower order harmonics

are eliminated using two unequal DC voltages for H-bridges. Multilevel Inverter has been recognized as an attractive topology for high voltage DC-AC conversion. Several multilevel topologies are reported and the most popular topology is Cascaded H-Bridge Multilevel Inverter. Normally, each phase of a cascaded H-Bridge multilevel inverter requires "n" DC sources for 2n+1 level. For many applications, multiple DC sources are required demanding long cables and this could lead to voltage unbalance among the DC sources [4]. With an aim to reduce the number of DC sources required for the cascaded H-Bridge multilevel inverter for a motor drive, this paper focuses on asymmetric cascaded H-Bridge multilevel inverter that uses two unequal DC sources in each phase to generate a five level equal step multilevel output. Multilevel voltage source inverter is recognized as an important alternative to the normal two level voltage source inverter especially in high voltage application. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverter. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this project, it is proposed to employ a new technique to obtain a multilevel output using less number of power semiconductor switches when compared to ordinary cascaded multilevel inverter. In the last decade, many researches were works continue for improving the performance of the Induction Motor. The induction motor accepted in variable speed drives due to its distinguished advantages of easy construction as well as low cost machine. The asynchronous machine uses some internal parts that need maintenance or replacement. The control voltage applied to the asynchronous machine can transforms the expression of electromagnetic torque of the asynchronous machine to practically the torque of the D.C. machine. In this work, the decoupling Vds and Vqs to control the flux particularly in the course of the component Ids and Iqs, which sharps to the suggestions of decoupling of the dependent excited D.C motor. The estimators determine the couple, the junction temperature, rotor flux and the stator pulsation. The control of induction motor can transform the expression of electromagnetic torque of to nearly the torque of the DC machine. An application of multilevel PWM inverter with microcontroller. Moreover, with multi level inverter PWM and application of rotor flux, the voltage applied to the IM solicits a modulator stage. This stage adds to the signal processing (orders IGBTs of the inverter of the type H) time and consequently limits the reactions of the control system, and hence the torque and speed response time. Also a hardware implementation of multilevel convertor with microcontroller control methodology for single phase induction motor system and its implementation in term of programming and code in real time operating system [5].

II. CASCADED H-BRIDGE MULTI LEVEL PWM INVERTER

The cascaded multilevel inverter consists of a series of H-bridge inverter. The general purpose of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, like batteries, fuel cells, solar cells, and ultra capacitors. Fig. 2 shows a single-phase structure of a cascade inverter with separate dc sources [5]. Each separate dc source is connected to a single-phase full-bridge inverter. The proposed cascaded multilevel inverter consists of two H-bridges. The first bridge H1 consists of a separate DC source Vdc, whereas the second bridge H_2 consists of a DC source 0.5Vdc as shown in Fig.1. Let the output of H-Bridge-1 be denoted as $v_1(t)$ and the output of H-Bridge-2 be denoted as $v_2(t)$. Hence the total output voltage is given by $v(t)= v_1(t)+v_2(t)$.By alternately opening and closing the switches S_1,S_4 and S_2,S_3 of H-Bridge- 1 appropriately, output of H1 v1(t) can be made equal to +Vdc, 0 or -Vdc. Similarly the output voltage of H-Bridge-2 $v_2(t)$ can be made equal to –0.5Vdc/, 0 or + 0.5Vdc by opening and closing the switches of H_2 [6]. Hence v(t) takes values–1.5Vdc,-Vdc,-0.5Vdc,0,+0.5Vdc,+Vdc,+1.5Vdc which are the five levels as shown in the Fig.2. The output voltage of the cascaded H-Bridge multilevel inverter is by:

$$v(t) = v_1(t) + v_2(t) \quad \text{... (1)}$$

i) Harmonics: The switching angles of the waveform will be adjusted to obtain the lowest output voltage THD. The harmonics orders and magnitude are depends up on the type of inverter and the control techniques. For example in single phase VSI, the output voltage waveform typically consists only of odd harmonics. The even harmonics are not present due to the half wave symmetry of the output voltage harmonics. The harmonic spectra depend on the switching frequency and the control method [6].

ii) Switching control of the inverter: There are number of modulation control techniques such as sinusoidal PWM method (SPWM) [7-11], space vector PWM method (SVPWM), selective harmonic elimination method (SHE) [12-14], and active harmonic elimination method [15], and they all can be used for inverter modulation control. For the proposed inverter control, a sensible modulation control method is the fundamental frequency switching control for high output voltage and Sinusoidal PWM control for low output voltage. In this paper, fundamental frequency switching control is used in H-bridge MLI [16].

The multilevel PWM inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages in stepped waveform. The commutation of the switches allows the addition of the capacitor voltages which reaches the high voltage level at

the output, while the power semiconductors withstand only with reduced voltage. A single phase leg of inverter with different numbers of levels by which the action of the power semiconductors is represented by an ideal switch with several positions. A five-level PWM inverter generates an output voltage with five values (levels) with respect to the negative terminal of the capacitor. By considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the Number of steps in the voltage between two phases of the load k is defined by:

$$K = 2m + 1 \quad \ldots(1)$$

The number of steps p in the phase voltage of a single-phase load in wyes connection is given by:

$$p = 2k + 1 \quad \ldots(2)$$

The term multilevel starts with the three-level inverter. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveforms, it results to reduction in harmonic distortion. However, a high number of levels results to increase the complexity and also it introduce voltage imbalance problems [1].

Three different topologies have been proposed for multilevel inverters as diode-clamped (neutral-clamped), capacitor- Clamped (flying capacitors) and cascaded multi cell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: Multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination and space-vector modulation (SVM).

The most attractive features of multilevel inverters are as follows:

1) It can generate output voltage with extremely low distortion.

2) It draws input current with very low distortion.

3) It generates smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, by using sophisticated modulation methods, CM voltages can be eliminated [8].

4) They can operate with a lower switching frequency.

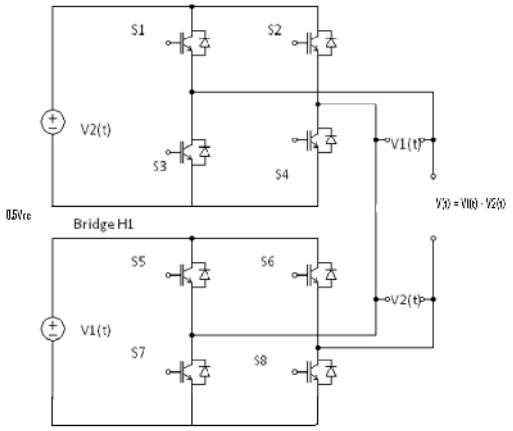

Fig.1. Cascaded H-Bridge multilevel PWM inverter.

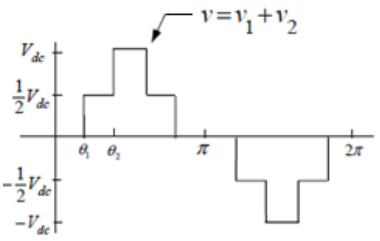

Fig. 2. Fundamental frequency waveform.

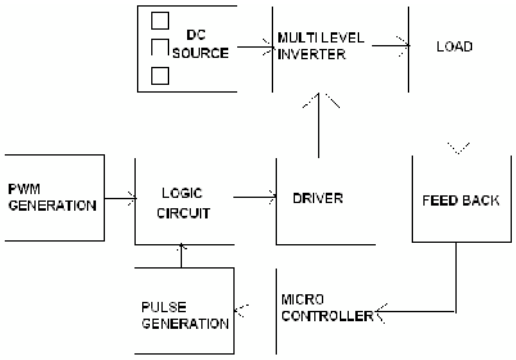

Fig. 3. Block diagram of proposed cascaded H-Bridge multilevel PWM inverter.

The early forms of DC to AC conversion are derived from the basic buck converter, where a power semiconductor is used to switch a DC signal into a square wave (Square Wave Inverter). With the introduction of power storage components, such as inductors and capacitors, this square wave will resemble a rough sinusoidal wave. The desired sinusoidal output can be further refined with the use of logic control on the semiconductors. It enables the positive and negative peaks of the square wave to be delayed (Phase Shifted Square Wave inverters), by creating a zero level. All these adjustment were made in the aid of producing a perfect sinusoidal output or in other words to decrease the Total Harmonic Distortion (THD) [38].

The PWM inverter further refine the conversion of the DC input to an AC output [21]. This advancement in inverter was not possible until recent semiconductor technology advancements. In this particular project, the semiconductors must have a high power rating combined with a high switching frequency. PWM inverters use high-speed semiconductor switches to switch the DC signal at varied time intervals, this will create varied pulse widths, hence the name Pulse Width Modulator [5-6].

Table 1. Conduction Sequence for Asymmetric Cascaded Multilevel Inverter.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	OUTPUT
1	0	0	1	0	0	1	1	$0.5V_{DC}$
0	0	1	1	1	0	0	1	V_{DC}
1	0	0	1	1	0	0	1	$1.5\ V_{DC}$
0	0	1	1	1	0	0	1	V_{DC}
1	0	0	1	0	0	1	1	$0.5\ V_{DC}$
0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	1	1	$-0.5\ V_{DC}$
0	0	1	1	0	1	1	0	$-\ V_{DC}$
0	1	1	0	0	1	1	0	$-1.5\ V_{DC}$
0	0	1	1	0	1	1	0	$-\ V_{DC}$
0	1	1	0	0	0	1	1	$-0.5\ V_{DC}$

Three voltage levels can be obtain using 2 voltage sources and two h bridges. If V_{dc} is the voltage of first h bride h1 then second h bride h2 is supplied 0.5 of Vdc. appropriate IGBT are switched on in order to get different voltage level. 0.5 Vdc, Vdc, 1.5 Vdc, 0. Which are repeated continuity and IGBT sequence is inverted for negative values.

Merits and Demerits:

Merits:

1. The series structure allows a scalable, modularized circuit layout and packaging since each bridge has the same structure.
2. Switching redundancy for inner voltage level is possible because the phase voltage output sum of each bridges output.
3. Potential of electrical shock is reduced due to separate DC sources.
4. Requires less number of components when compared to other two types.
5. Device voltage sharing is automatic because of the independent DC supplies. There is no restriction on switching pattern.
6. With N devices (each capable of operating at voltage V_{dc}) per-phase, the circuit can produce an output varying between $\pm(N/2)*(V_{dc}/2)$. By using a lot of H-bridges, very high voltage converters can be made this way.
7. The circuit is modular –this is an advantage for manufacture and maintenance.

Demerits:

1. Limited to certain applications where separate DC sources are available.
2. Usage of the power semiconductor switches increases exponentially whenever the level is to be increased.
3. Each H-bridge needs an isolated DC supply compared to the other solutions which need only one supply.

III. HARDWARE IMPLEMENTATION

To Capture and Compare the PWM modules a version of the modulator suitable for the voltage control, accepts as:

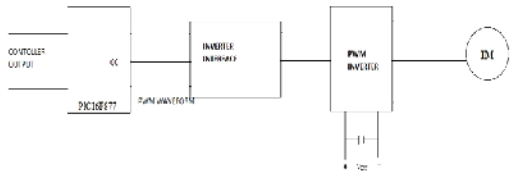

Fig. 4. Block diagram of the used system to test the modulator.

Inputs the voltage demand in dq stator coordinates (U, and U), and generates the on-line single-phase PWM digital waveforms, which drive the power stages [18]. In the proposed solution, the modulator hardware is just a 8-bit microcontroller with minimum additional logic, which provides the interface with power stage. The microcontroller is a 16F877A. Microcontroller for specially designed for complex, real-time control applications [37]. It shares a common, register-based architecture core that eliminates the accumulator bottleneck and enables fast context switching. Although the 16F877A. Microcontrollers are a 8-bit architecture, all devices have bit, byte, word and 8-bit operations. The Motion Control family has peripherals that are optimized for single-phase AC induction motor control and power inverter applications. These devices have a unique peripheral, the capture and compare module (CCM), which really simplifies the control with 5 level PWM inverter gate driver circuit and external hardware used for generating single-phase pulse width modulation waveforms. The capture and compare module (CCM) generates three complementary. On-overlapping PWM pulses with resolutions of 250 ns (with a 16 MHz oscillator). Once initialized, the CCM require to change PWM duty cycles. The CCM features programmable switching (or carrier) frequency up to 1 kHz, duty cycle and dead time. The dead time generator (included in the CCM peripheral) prevents the complementary outputs from being turned on at the same time, in order to avoid a short circuit in one leg of the power inverter. This peripheral also has all programmable high drive capability outputs for each phase. The outputs have programmable polarity, or may be forced high or low. Fig. shows how the CCM produces the PWM waveforms. The CC-COUNTER register determines the switching frequency.

The CC-COUNTER register is a 8-bit counter which is clocked every state machine. When the counter is running, it continuously counts up and down between OOOlH and the CC-RELOAD value.

When the counter equals the Capture and compare module (CCM)s (there are three Capture and compare module (CCM)s, one for each phase) the outputs are complemented, so, this register set the pulse width. Each time the CC-COUNTER register reaches the CC-RELOAD value, an interrupt is generated (PI-Interrupt). This interrupt is used to change,, the CC-COMP register values (if needed). [Specification of capture and compare module

- Capture is 16-bit, max. Resolution is 12.5 ns
- Compare is 16-bit, max. Resolution is 200 ns
- PWM max. Resolution is 10-bit

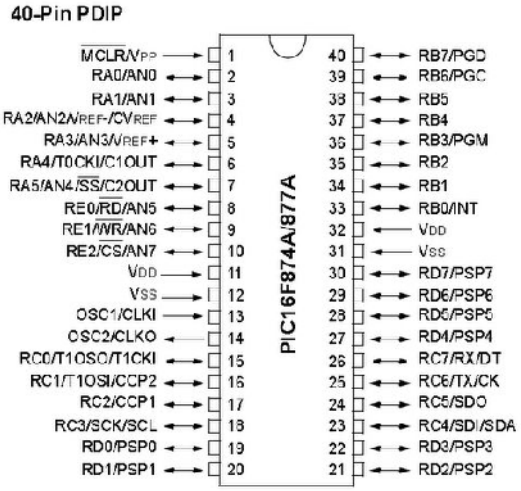

Fig. 5. Pin description of PIC16F877A.

IV. SOFTWARE IMPLEMENTATION

The general flowchart of the modulator software design is shown in Fig. 7. There are basically two concurrent tasks: the main routine and ISR (Interrupt Service Routine). In the main routine the port c, inputs to the IGBT gate driver circuit produced by the controller, are used, firstly, we determine the IGBT combination to be switched ON and output values to the corresponding port C which is connected too gate driver circuit. After each PWM counter next combination is switched ON. In this way all combination are output too generated multi level wave form for the motor. For other two phase120 phase shifted output is generated. The minimum pulse width resolution is 250 ns, independently of the CC-RELOAD value. The actual resolution depends on the carrier frequency selected: the higher the carrier frequency, the worst the pulse width resolution.

The carrier frequency used in the experiments was about 1 kHz, which allows a pulse width resolution of 1/256, perfectly acceptable for most applications. With this frequency the switching times are updated within one carrier periods. The modulator synthesizes a frequency in the range of 0 Hz to 70 Hz [3].

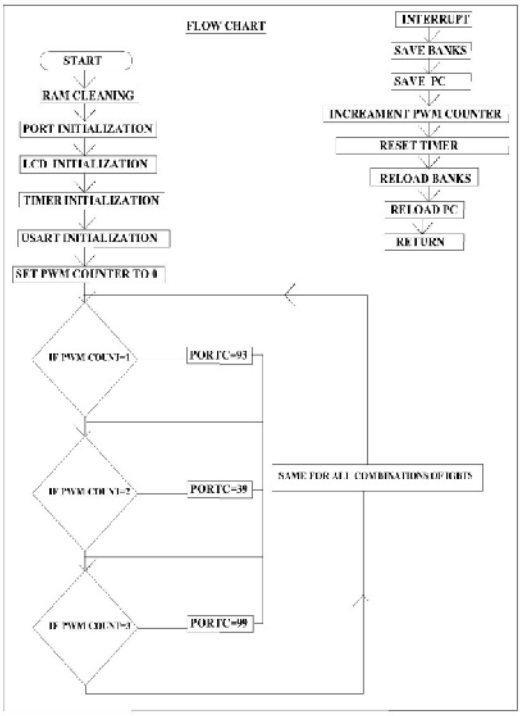

Fig. 6. Flowchart of software deign.

V. EXPERIMENTAL RESULTS

To experimentally validate the proposed cascaded H-bridge multilevel inverter, a prototype single-phase cascaded H-Bridge multilevel converter has been built using IGBTs as switching device. In this paper the hardware is implemented using the PIC microcontroller PIC16F877. The advantages of the PIC microcontroller is that the instruction set of this controller are fewer than the usual microcontroller. U unlike conventional processors, which are generally complex, instruction set computer (CISC) type, PIC microcontroller is a RISC processor. The advantages of RISC processor against CISC processor are RISC instructions are simpler and consequently operate faster A RISC processor takes a single cycle for each instruction , while CISC processor requires multiple clocks per instruction (typically, at least three cycles of the rough put execution time for the simplest instruction 12 to 24 clock cycles for more complex instructions), which makes decoding a tough task, and the control unit

in a CISC is always implemented by a micro-controller which is much slower than the hardware implemented in RISC. Overall the RISC processor can provide processing power more than three times of a CISC processor in a particular field of application PIC16F877 microcontroller is used to generate triggering pulse for IGTs. It is used to control the output of the inverters.

Micro controller have more advantage compare then analog circuits and micro processor such as fast response, low cost, small size and etc. Driver is also called as power amplifier because it is used to amplify the pulse output from micro controller. It is also called as opt coupler IC. It provides isolation between microcontroller and power circuits. The PIC16F84A belongs to the mid-range family of the PIC microcontroller devices.. 0.5 hp induction motor is connected to the system and successfully run using 5level inverter techniques .the supply voltage under take is 100V maximum in total. The motor is tested under no load condition. The hardware and power components run in under operating temperature in normal and industrial environment. Different input voltages are applied to check the motor performance for suitable running with the help of solar power as input source in further uses.

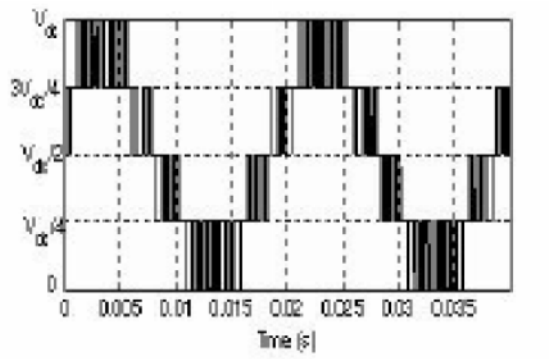

Fig. 7. Experimental generated 5-level wave form of PWM inverter.

VI. CONCLUSION

In this paper the sinusoidal PWM scheme is used for modulation control. In cascaded H-bridge multilevel inverter separated unequal DC sources are used to generate sinusoidal output. A fundamental switching scheme is used and produces a nearly sinusoidal output. This cascaded inverter design is to get the improved sinusoidal output of an inverter and gives less THD%. The elimination of harmonics in a cascade H-bridge multilevel inverter by considers the inequality of separated dc source. The PWM techniques have been analyzed for the cascaded H-Bridge multilevel inverter. A Micro-controller based gating circuit generates. the pulses required by the inverter. The induction motor drive system is successfully fabricated and tested. This can be important in the high power quality cascaded multilevel inverters which require several voltage sources and knowledge of the dc voltage levels. Applications of the cascaded multilevel inverter include Naval ship propulsion which necessitates high power quality. A PWM modulator, suitable for voltage control, was presented and tested with a 0.5 H.P. single-phase induction motor fed by an IGBT 5-level PWM inverter [40-48].

The proposed solution was based on a high performance 8-bit microcontroller with gate driver circuit and additional hardware.

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